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(54) A package for a semiconductor device

(57) A package for an integrated circuit includes a circuit board 122 for mounting the integrated circuit 114 having a first surface and a second surface, a connection device positioned on the first surface of the circuit board 122 for electrically connecting the integrated circuit 114 and the integrated circuit 114 being positioned on the second surface of the integrated circuit 114.

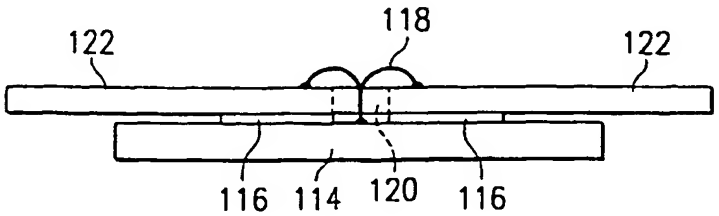

FIG. 13

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Description

TECHNICAL FIELD OF THE INVENTION

The present invention relates to semiconductor devices, and more particularly to packaging board on chip (BOC) devices.

BACKGROUND OF THE INVENTION

The semiconductor technology has shown a general trend towards the dramatic increase in integrated circuit speed and density. Both of these trends are fueled by a general reduction in device (active element) geometries. As semiconductor devices becomes smaller, the distances between devices on a semiconductor die become smaller, and parasitics (such as parasitic capacitances) and switching currents become smaller. In technologies, such as CMOS, where overall current draw and switching speed characteristics are dominated by the effects of parasitics, the result is a reduction in total power consumption at the same time as switching speed is improved. Overall speed is further improved by the reduction in signal propagation time between active devices (e.g., transistors), resulting from the shorter distances involved. In today's high speed integrated circuitry based on sub-micron geometries, delays in the tens or hundreds of picoseconds can be appreciable.

Typically, integrated circuit dies (chips, or semiconductor dies) are diced (cut apart, or singulated) from a semiconductor wafer and are separated into integrated circuit packages which have pins, leads, solder (ball) bumps, or conductive pads by which electrical connections may be made from external systems to the integrated circuit chip. These packages are then typically applied to circuit board assemblies including systems of interconnected integrated circuit chips.

The aforementioned dramatic improvements in integrated circuit speed and density have placed new demands on integrated circuit assemblies, both at the chip and circuit board levels. Without attendant improvements in these areas, much of the benefit of high device speed is lost. Wiring propagation delays and transmission line effects, in integrated circuit packages and on circuit board assemblies, which were once negligible are now significant factors in the overall performance of systems based on high-speed integrated circuitry. In order to achieve the potential higher system level performance opportunities afforded by the new high density technologies, it is necessary to reduce the amount of signal propagation time between integrated circuits.

Another significant factor in achieving high system level performance is signal drive capability. Longer signal paths are susceptible to noise, cross-talk, etc., and require low impedance, high current drive circuits on the integrated circuit chips (dies). Such circuits tend to occupy large portions of the die area, either reducing the area available for other circuitry or increasing the overall die size, and can introduce significant delays of their own. Clearly, shorter signal paths and their attendant low signal drive current requirements are desirable to achieve high performance.

In the prior art, a number of high density chip assemblies and packages have been proposed and implemented. One such technique is commonly known as "chip-on-board" technology, whereby integrated circuit dies are bonded directly to die mounting areas on a circuit board substrate, for example, ceramic, fiberglass, etc., and are wire bonded (with thin "bond wires") to traces on the circuit board in areas adjacent to the edges of the dies. The elimination of the traditional integrated circuit package permits chips to be placed much closer together than would otherwise be possible, thereby shortening signal paths and reducing delays.

SUMMARY OF THE INVENTION

The present invention reduces inductance that is induced between wires and internal leads. Additionally, the present packaging arrangement provides one package for all applications. The package for the present invention provides short traces leading to favorable impedance coupling. These short wires are designed to reduce electrical impedance important for the operation of high speed devices, such as the synchronous DRAM. Additionally, the present invention eliminates wire shorts to the bus bar and eliminates T/F. Additionally, the present invention eliminates the use of ultra-advance molding equipment development. Additionally, the present invention provides a true chip size package, which leads to improved mapping density. Additionally, the present invention eliminates bent leads. Lastly, the present invention eliminate noise due to cross-talk and improves the delays associated with longer wires.

The present invention includes a package for an integrated circuit, including a circuit board for mounting the integrated circuit having a first surface and a second surface, a connector device positioned on the first surface of the circuit board for electrically connecting the integrated circuit, and the integrated circuit being positioned on the second surface.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described, by way of example, with reference to the accompanying drawings in which;-

Fig. 1 illustrates a sideview of package die with potting topside;

Fig. 2 illustrates a topview of the package with a stitch design;

Fig. 3 illustrates a sideview of another package die with molding topside;

Fig. 4 illustrates the topview of the same package die;

Fig. 5 illustrates another package die with molded topside;

Fig. 6 illustrates a variation of the package of Fig. 5 with potter topside;

Fig. 7 illustrates another sideview of another package with potter topside;

Fig. 8 illustrates another sideview of another package die with molding topside;

Fig. 9 illustrates the board and solder bumps; and

Figs. 10-14 illustrates a process of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 illustrates that solder balls 100 are positioned along the longitudinal edges of printed circuit board 122. To provide the maximum spacing between the individual solder balls, the solder balls may be positioned along the outer edges of the printed circuit board 122. The number of the solder balls 100 correspond to the number of connections to the semiconductor die 114. The semiconductor die 114, which has been previously cut or diced is mounted to the printed circuit board 122 by an attachment apparatus, for example, polymide tape or any adhesive material suitable to attach the semiconductor die 114 to the printed circuit board 122. Advantageously, the semiconductor die 114 is the type with connections along the longitudinal axis of the semiconductor die. The electrical connection may be positioned along the central axis of the semiconductor die 114. The solder balls 100 are connected to the semiconductor die 114 by wires 118 which may be made of material gold and traces (not shown). These wires 118 are attached to the semiconductor die on the side of the semiconductor die 114 that faces or abuts the printed circuit board 122. The wires 118 extend from the semiconductor die 114 through a hole 120 of the printed circuit board and are attached to traces which run along or through the printed circuit board to the solder balls. The hole through the printed circuit board 122 may be positioned at the central longitudinal axis of the printed circuit. The semiconductor die 114 and wires 118 are protected from external objects by the elements by sealing material, such as the epoxy resin to form the chip-on-board (COB) semiconductor device. Although, top and bottom have no absolute meaning, for purposes of this application, the side of the printed circuit board 122 with the solder balls 100 and away from the semiconductor die 114 is referred to as the top portion while the bottom portion of the printed circuit board 122 is the side opposite to the solder balls 100 and the same side as the semiconductor die 114.

The sealing material 110, which is formed on the top surface of the printed circuit board 114 to cover the wires 118 and the hole 120 protects the wires and has a general curved shape. The bottom sealing material 112 forms between the printed circuit board 122 and the semiconductor die 114 to encapsulate the adhesive means 116 and the wires 118 and further encapsulate the sides of the semiconductor die 114. The bottom of the bottom sealing material 112 is approximately flush with the bottom of the semiconductor die 114.

Fig. 2 illustrates that the top sealing material 110 is formed around the wires 118 and are generally perpendicular to the longitudinal axis of the printed circuit board 122. The height of the packaged device is very compact and approximately only 42 mils. The wires 118 are very short and eliminate inductance. The height between the bottom of the printed circuit board 122 and the bottom of the semiconductor die 114 is approximately 14 mils while the height from the top of the printed circuit board 122 to the top of the solder balls 100 is approximately 20 mils. The semiconductor die 114 is spaced approximately 1 to 3 mils from the bottom of the printed circuit board 122 depending on the type of die attached used.

Fig. 3 illustrates a variation of the package of Figs. 1 and 2, in that the top sealing material 124 has more angular shape with sloping sidewalls. The topview of Figure 4 illustrates that the sealing material 124 has an approximately rectangle shape.

Fig. 5 illustrates that the bottom sealing material 126 is not flush with the bottom of the semiconductor die 114 and entirely encapsulates the semiconductor die 114 including the bottom surface of the semiconductor die 114. This improves the protection of the semiconductor die 114, but increases the overall height to approximately 50 mils.

Fig. 6 illustrates that the top sealing material is a curved top sealing material 110. The overall height of this package is approximately 50 mils.

Fig. 7 illustrates that the semiconductor die 114 is not enclosed on either the bottom or sides by a sealing material. The adhesive material 116 extends from the hole 120 to the outermost side of the printed circuit board 122. This extension of the adhesive material 116 provides a stable mounting platform for the semiconductor die 114.

In Fig. 8, the angular top sealing material 124 is used with the extended adhesive material 116. The dimensions ot the semiconductor die 114 are approximately the same as the printed circuit board 122 along the longitudinal axis of the printed circuit board 122.

Fig. 9 illustrates a construction in the form of a structure of the printed circuit board 122 with the solder balls. The structure includes a hole 200 formed by etching, ion milling or other suitable process and extends from the top surface of the printed circuit board 122 into the printed circuit board 122 down to and exposing conductor

202. Insulating material 204, for example, SIO_2, electrically insulates the walls of the hole 200 from contact with other active semiconductor devices or different wires 118 of the same semiconductor device. A conductive plug 206 is deposited in to hole 200 forming a conductive via from the surface of the printed circuit board 122 to the conductor 202. Contact 208 is electrically conductive to plug 206 and is formed on the top surface of the printed circuit board.

Figs. 10-14 illustrates a process for the construction of device in accordance with the principals of the present invention.

A hole 120 is formed along the central longitudinal axis of the printed circuit board 122. Adjacent to the hole 120 and on the bottomside of the printed circuit board 122, adhesive material 116 is placed. Semiconductor die 114 is positioned next on the adhesive means 116 as illustrated in Fig. 12.

In Fig. 13, wires 118 are formed from the semiconductor die 114 to the conductors located in the printed circuit board 122 by wire bonding machines (not shown). As illustrated in Fig. 14, a top sealing material 124 protects the wires while a bottom sealing material 126 protects the semiconductor die. These top and bottom sealing materials are formed by molding machine (not shown). Thus, the wires are very short and eliminate inductance resulting from longer wires and provides favorable impedance and coupling to the semiconductor die. Furthermore, no bus bar is needed.

The present invention further eliminates or minimizes bent leads resulting from the wire placement process.

Claims

1. A package for an integrated circuit, comprising:

   means for mounting the integrated circuit having a first surface and a second surface;
   a connector device positioned on the first surface for electrically connecting the integrated circuit; and
   said integrated circuit being positioned on the second surface.

2. A package for an integrated circuit as in Claim 1, wherein said integrated circuit is attached to said second surface by epoxy.

3. A package for an integrated circuit as in Claim 1, wherein said integrated circuit is attached to said second surface by adhesive tape.

4. A package for an integrated circuit as in Claim 3, wherein said adhesive tape is polymide tape.

5. A package for an integrated circuit as in any preceding Claim, wherein said means comprises a hole therethrough for placing wires to connect the integrated circuit and said connection device.

6. A package for an integrated circuit as in any preceding Claim, wherein said connection device includes a solder ball.

7. A package for an integrated circuit as in any preceding Claim, wherein the package further comprises:

   a sealing material to seal the integrated circuit, and wherein the sealing material forms a flush surface with a surface of the integrated circuit.

8. A package for an integrated circuit as in any preceding Claim, wherein the package further comprises a sealing material for encapsulating the integrated circuit.

9. A package for an integrated circuit as in any preceding claim, wherein said means for mounting the integrated circuit is a circuit board.

10. A method of forming a package for an integrated circuit comprising;

    forming a hole through a circuit board having a first surface and a second surface;
    placing a connector device on the first surface adjacent said hole for electrically connecting the integrated circuit;
    placing said integrated circuit on the second surface in the region overlaying said hole.

11. The method of claim 10, further comprising securing said integrated to said second surtace by means of an adhesive.

12. The method of Claim 10 or Claim 11 further comprising forming wires from said integrated circuit to said first surface through said hole.

13. The method of any of Claims 10 to 12 further comprising forming a sealing material over said hole and a region of said first surface adjacent said hole.

14. The method of any of Claims 10 to 13 further comprising forming a sealing material over said integrated circuit.

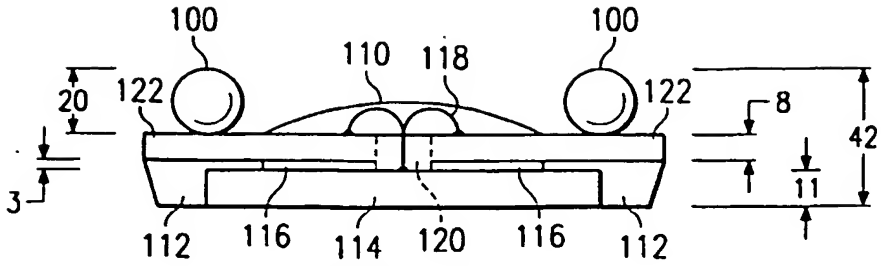


FIG. 1

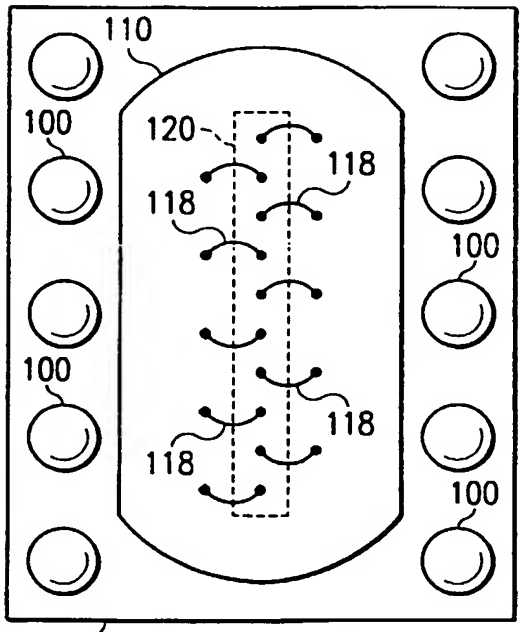


FIG. 2

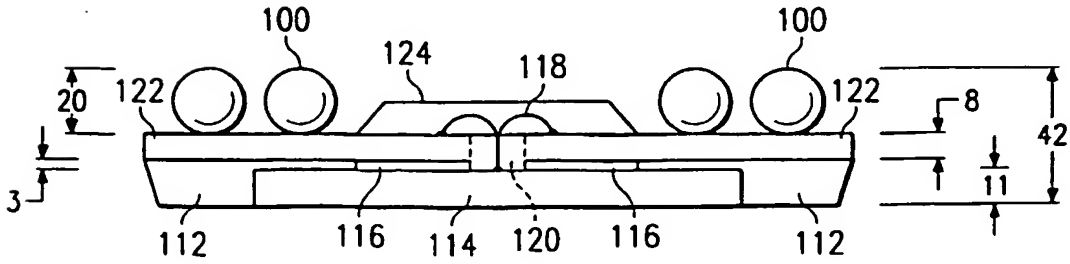


FIG. 3

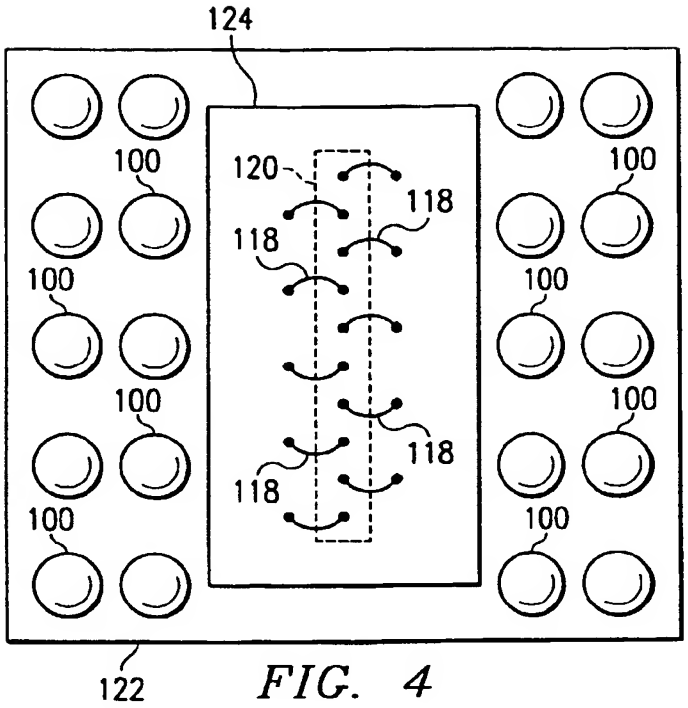


FIG. 4

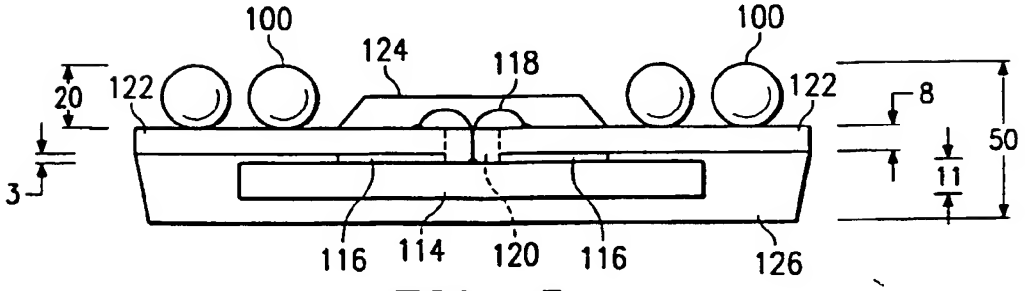


FIG. 5

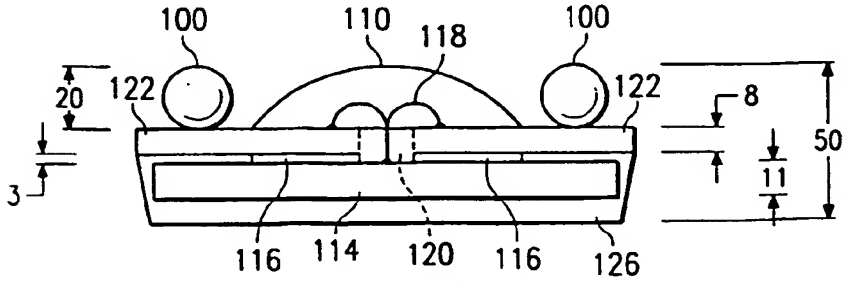


FIG. 6

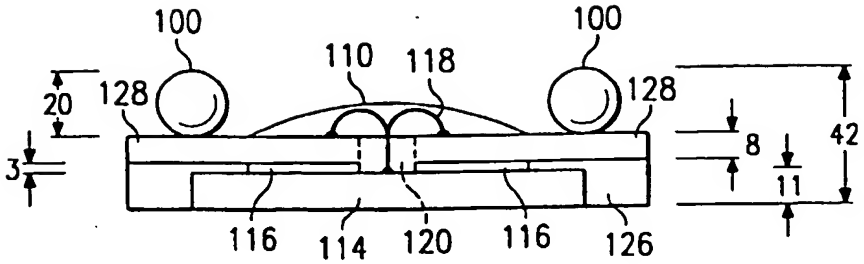


FIG. 7

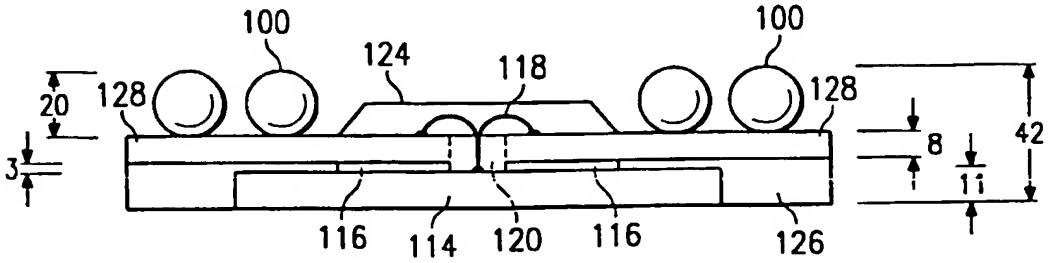


FIG. 8

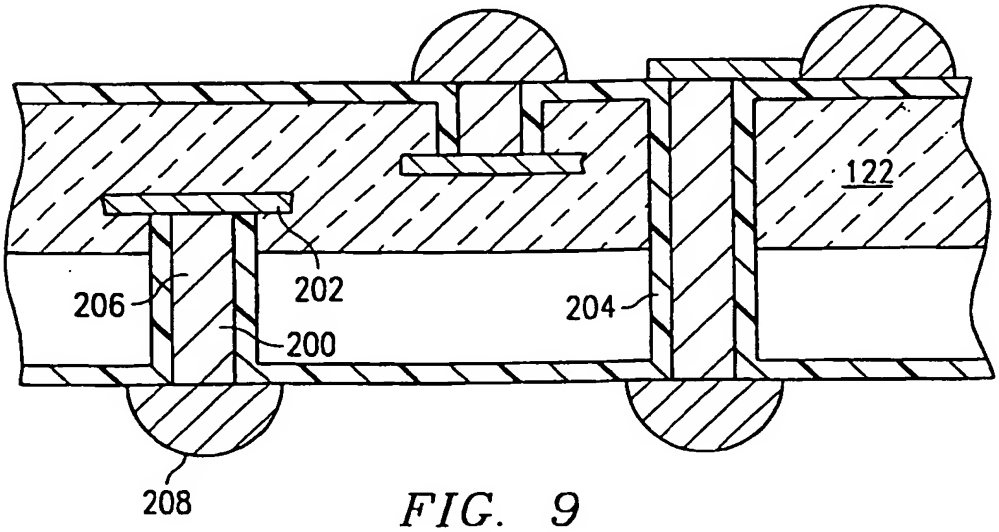


FIG. 9

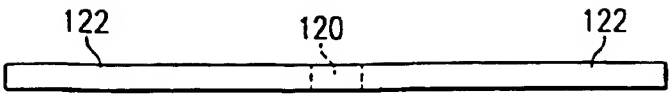


FIG. 10

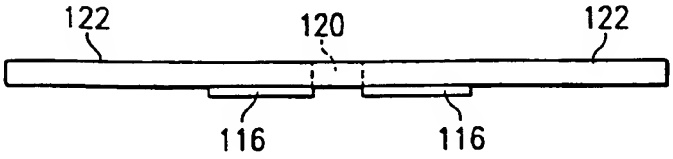


FIG. 11

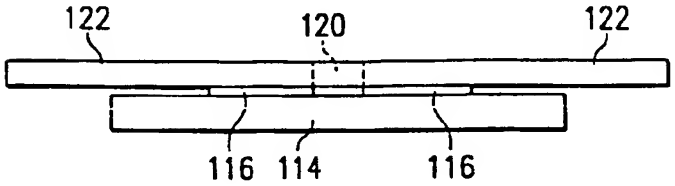
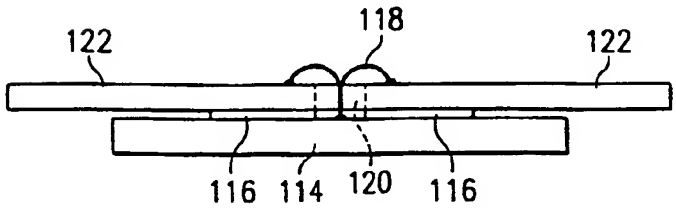


FIG. 12



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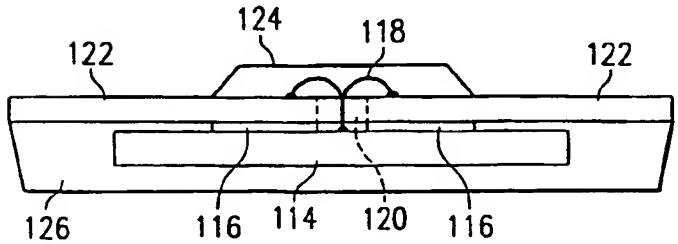

FIG. 14

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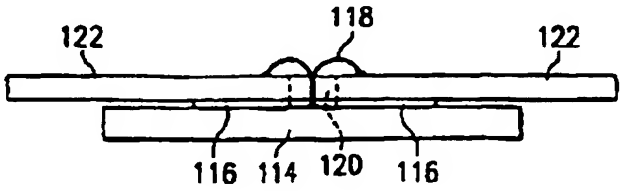

FIG. 13

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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 3638

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IntCl.6)
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X	PATENT ABSTRACTS OF JAPAN vol. 008, no. 013 (E-222), 20 January 1984 (1984-01-20) -& JP 58 178529 A (MITSUBISHI DENKI KK), 19 October 1983 (1983-10-19) * abstract *	1,2,5,7, 9-13	
X	EP 0 698 920 A (TEXAS INSTRUMENTS INC ;TEXAS INSTRUMENTS ITALIA SPA (IT)) 28 February 1996 (1996-02-28) * page 3, column 3, line 16 - column 4, line 30; claims 1-5; figure 2 *	1,3-5,8, 10-14	
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 004, 30 April 1996 (1996-04-30) -& JP 07 321244 A (MATSUSHITA ELECTRIC IND CO LTD), 8 December 1995 (1995-12-08) * abstract; figures 1,3,5A,5B,6A-6C *	1,5-7,9, 10,12,13	TECHNICAL FIELDS SEARCHED (IntCl.6) H01L
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 August 1999	ZEISLER, P

CATEGORY OF CITED DOCUMENTS

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